

LA-UR-21-23411

Approved for public release; distribution is unlimited.

Title: HSADC FMC

Author(s): Weaver, Charles T.

Intended for: Share with industry

Issued: 2021-04-09

Disclaimer:

Los Alamos National Laboratory, an affirmative action/equal opportunity employer, is operated by Triad National Security, LLC for the National Nuclear Security Administration of U.S. Department of Energy under contract 89233218CNA000001. By approving this article, the publisher recognizes that the U.S. Government retains nonexclusive, royalty-free license to publish or reproduce the published form of this contribution, or to allow others to do so, for U.S. Government purposes. Los Alamos National Laboratory requests that the publisher identify this article as work performed under the auspices of the U.S. Department of Energy. Los Alamos National Laboratory strongly supports academic freedom and a researcher's right to publish; as an institution, however, the Laboratory does not endorse the viewpoint of a publication or guarantee its technical correctness.



HSADC FMC

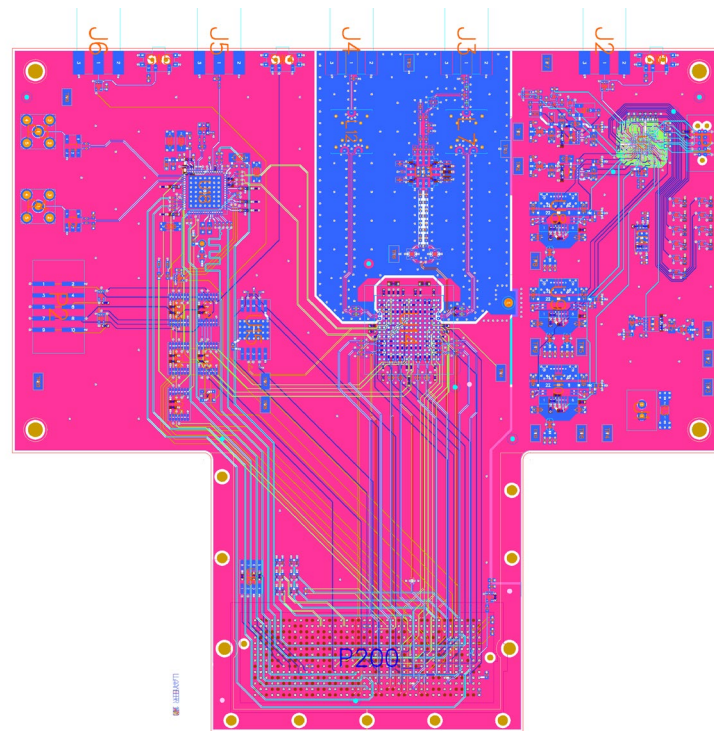
Charley Weaver, ISR-4

4/6/2021

LA-UR-XX-XXXXX

Concept: Space Grade ADC in FMC+ Form Factor

- Radiation hardened A/D converter
 - For use in GEO / MEO / LEO Orbits
 - 100 krad TID minimum
 - Latch-up immune to 103 MeV-cm²/mg
 - JESD204B interface
 - Multi-gigahertz sample rates
 - MIL-PRF-38535 Class Q/V
- Industry standard VITA 57.4 FMC+
 - Standard mezzanine card form factor and connectors
 - Modular interface to an FPGA located on a base board
 - Multi-gigabit SERDES support



Layout and Routing



HSADC Features

- The central component to the design is a high speed analog-to-digital converter from Texas Instruments, part number ADC12DJ3200QML-SP.
- JESD modes (JMODEs): determines the operation of the ADC via SPI registers. The JMODE should be determined for each individual application. For example, choosing JMODE 9 will give the user two channels, 15-bit samples per channel, and use 8 SERDES lanes.
- The radiation performance for the ADC is 300 krad TID, a single-event latchup spec. of 120 MeV-cm²/mg, and SEU immune registers.
- Power Consumption: 3W

ADC JMODEs	
# of modes	18
Resolution	8 to 15 bit
Decimation	None, /2, /4, /8, /16
Sample Rate	0.05 to 6.4 GSPS
SERDES	1 to 16 lanes
Optional DDCs w/ complex output	



HSADC FMC Prototype

- Initial design extends the FMC+ standard board outline
 - Prototype testing requires additional board space used for optional circuits
- Example: one channel has optional DC coupling, variable gain, attenuation, and filtering
- Design can be revised for individual applications to fit standard form factor
- HSADC FMC power estimate: 6.5W

